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Electrical Characterization of RF Reactive Sputtered p–Mg-$In_xGa_{1-x}N$/n–Si Hetero-Junction Diodes without Using Buffer Layer

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Abstract: The modeling of p–$In_xGa_{1-x}N$/n–Si hetero junction diodes without using the buffer layer were investigated with the "top-top" electrode. The p–Mg-GaN and p–Mg-$In_{0.05}Ga_{0.95}N$ were deposited directly on the n–Si (100) wafer by the RF reactive sputtering at 400 °C with single cermet targets. Al and Pt with the square size of 1 mm^2 were used for electrodes of p–$In_xGa_{1-x}N$/n–Si diodes. Both devices had been designed to prove the p-type performance of 10% Mg-doped in GaN and InGaN films. By Hall measurement at the room temperature (RT), the holes concentration and mobility were determined to be $N_p = 3.45 \times 10^{16}$ cm^{-3} and $\mu = 145$ $cm^2/V{\cdot}s$ for p–GaN film, $N_p = 2.53 \times 10^{17}$ cm^{-3}, and $\mu = 45$ $cm^2/V{\cdot}s$ for p–InGaN film. By the I–V measurement at RT, the leakage currents at −5 V and turn-on voltages were found to be 9.31×10^{-7} A and 2.4 V for p–GaN/n–Si and 3.38×10^{-6} A and 1.5 V for p–InGaN/n–Si diode. The current densities at the forward bias of 20 V were 0.421 and 0.814 $A{\cdot}cm^{-2}$ for p–GaN/n–Si and p–InGaN/n–Si devices. The electrical properties were measured at the temperature range of 25 to 150 °C. By calculating based on the TE mode, Cheungs' and Norde methods, and other parameters of diodes were also determined and compared.

Keywords: p–Mg-InGaN films; RF sputtering; I–V measurement; Cheung's method; Norde's method; TE mode

1. Introduction

GaN and InGaN have excellent characteristics such as high conductivity and high mobility. The development and creation of p–layer GaN and InGaN materials involve one of the important technologies in designing electronic devices [1–5]. The investigation of high-quality doping in GaN and InGaN semiconductors by incorporating elements such as Zn, and Cu, Mg for p–GaN behavior, and its alloys had reported [4–8]. The success of Mg doping in forming p-$In_xGa_{1-x}N$ films is an important factor for developing electric devices, a photo detector, and solar cell devices [7–10]. Si wafer has often been used for the growth of GaN, InGaN, and their alloys for applications in photo-detector, solar cells, and electronic devices. The combination between n–InGaN layers and n–Si wafers were studied to improve the interface layers by using an assortment of approaches [11–14]. For fabricated electronic devices, the growth of the InGaN layer on n–Si wafers were studied to improve the interface layers by

using a variety of approaches [15–20]. Lee at al. studied electrical properties of a nanowire *n*–GaN/*p*–Si device by forming dielectrophoretic alignment. At the current density of 10–60 A/cm^2, the diode was well-defined with a forward voltage drop of 1.2–2.0 V and high resistance in the range of 447 KΩ [17]. Li et al. used the RF sputtering method to deposit the Mg-doped GaN films on the Si substrate and design the homo junction GaN diodes. By testing the *I–V* measurement, the turn-on voltages of diodes were 2.3 and 2.1 V for as-deposited and 500 °C-annealed sample, respectively [21]. Vinay Kabra et al. investigated the *p*–ZnO/*n*–Si hetero junction diode by using a dip coating technique. Their electrical properties showed the highly rectifying, with a rectification ratio of 101 at 3 V [22]. Mohd Yusoff et al. reported the *p*–*n* junction diode based on GaN grown on the AlN/Si (111) substrate and annealed samples at 700 °C. The ideality factors of their diodes decreased from 19.68 to 15.14, with the testing temperature increasing from 30 to 104 °C [23]. In previous work, the Mg–doped $In_xGa_{1-x}N$ films had been deposited on Si (100) substrates by RF reactive sputtering. The Mg–$In_xGa_{1-x}N$ films had the *p*–type conduction at $x \leq 0.075$. The *p*–Mg–$In_{0.05}Ga_{0.95}N$/*n*–GaN diode was shown the leakage current of 2.7×10^{-6} A, turn-on voltage of 1.8 V, and breakdown voltage of 6.8 V at the RT [12].

All previous groups often investigated the *p*–GaN films and their alloys by using MOCVD above 800 °C and other methods. The sputtered technique with the low temperature at and below 400 °C has been hardly declared. Furthermore, there is no report on the electrical properties of *p*–Mg-$In_xGa_{1-x}N$/*n*–Si diodes without using buffer layers. In this study, to prove the success of Mg doping in the *p*–GaN and the *p*–InGaN films, the modeling of *p*–Mg-$In_xGa_{1-x}N$/*n*–Si hetero junction diodes was designed by using the RF reactive sputtering. This method was chosen to design diodes due to the benefits of low sputtered-temperature, low cost, and safe working atmosphere [7,13,15]. The *n*–Si (100) wafer was also used for its low cost, large wafer size, and easy availability [18,22,24]. The electrical characteristics of devices were calculated by the thermionic emission (TE) mode at different testing temperatures [3,12,13].

2. Materials and Methods

Figure 1 shows the structural modeling of a *p*–$In_xGa_{1-x}N$/*n*–Si hetero junction diode. This device was designed on the *n*−Si (100) wafer by modeling with the "top-top" electrode. The *p*–Mg-$In_{0.05}Ga_{0.95}N$ and *p*–Mg-GaN films were deposited together on the *n*–Si (100) and SiO_2/Si (100) substrate. The *n*–Si (100) wafer had sheet resistance of ~1–10 Ω·cm, diameter of 2 inches, thickness of ~550 µm, and the polished surface. Sputtered-$In_xGa_{1-x}N$ films on SiO_2/Si substrate were used for testing Hall measurement and SEM analysis.

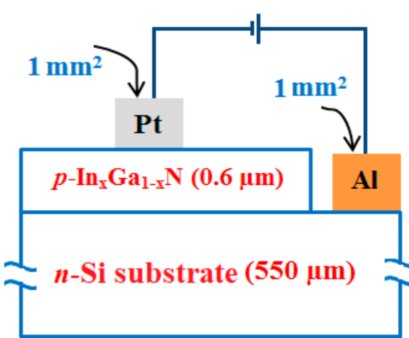

Figure 1. Structural modeling of *p*–$In_xGa_{1-x}N$/*n*–Si hetero junction diode.

For the *p*–GaN film, the sputtering cermet target was made by hot pressing with the mixture of metallic Mg, Ga powders, and GaN powder. The [Mg]/([Ga]+[Mg]) molar ratio in each cermet target was reserved at 10%. Similar for *p*–InGaN film, the [Mg]/([In]+[Ga]+[Mg]) molar ratio in each cermet target was also kept at 10%. The [In]/([In]+[Ga]+[Mg]) molar ratios was 5%. The *p*–Mg–$In_xGa_{1-x}N$ films (with x~0 and 0.05) were deposited on *n*–Si (100) substrates at 400 °C for 25 min by RF reactive

sputtering. Both Mg–$In_xGa_{1-x}N$ targets were sputtered with RF power of 150W under the gas mixture of Ar and N_2, which remained at 5 sccm for each.

The pure Aluminum (99.99%) and Platinum (99.99%) targets were used for making the electrodes for p–$In_xGa_{1-x}N$/n–Si hetero junction diodes. By using steel masks with the square size of 1 mm^2, these electrodes were deposited at 200 °C, with RF power of 80W for 30 min on top of p–$In_xGa_{1-x}N$ films and n–Si substrate. The detail procedure for creating the p–GaN and p–InGaN films, made by RF reactive sputtering, can be referred to our previous works [10–12,21].

In this work, our diodes were designed at the low sputtered-temperature and high pressure. The holes' concentration, electrical conductivities, and mobilities of p–Mg-$In_xGa_{1-x}N$ films and n–Si wafer were measured by a Hall measurement (HMS–2000, Ecopia, Tokyo, Japan). Scanning electron microscopy (SEM, JSM–6500F, JEOL, Tokyo, Japan) was used to observe the surface morphology of p–$In_xGa_{1-x}N$ films. Energy dispersive spectrometer (EDS, JSM–6500F) equipped on SEM was used for composition analysis of films. The *I*–*V* characteristics of p–$In_xGa_{1-x}N$/n–Si diodes were measured by using Semiconductor Device Analyzer (Agilent, B1500A, Tokyo, Japan) with the different temperature. All parameters of diodes were calculated by following the equations of the TE mode as well as the Cheungs' and Norde method.

3. Results and Discussion

3.1. Structural and Electrical Characteristics

The carrier concentration (N_p) and carrier mobility (μ) of n–Si wafer were found to be $N_p = 4.7 \times 10^{15}$ cm^{-3} and = 196 cm^2/V.s when measuring the Hall effect at room temperature (RT). The holes concentration (N_p) and mobility (μ) were also determined to be $N_p = 3.45 \times 10^{16}$ cm^{-3}, μ = 145 cm^2/V·s for p–GaN film, and $N_p = 2.53 \times 10^{17}$ cm^{-3}, μ = 45 cm^2/V·s for p–InGaN film, respectively. By SEM analysis, the thicknesses of Pt and Al layers were ~250 nm and the thickness of both p–$In_xGa_{1-x}N$ films was ~0.6 μm.

3.2. The Energy Band Diagram

Figure 2 displays the energy band diagram of a p–$In_{0.5}Ga_{0.95}N$/n–S*i* diode as an example. Our band gap (E_g) of Mg-doped $In_{0.5}Ga_{0.95}N$ (Mg of 10%) films at 400 °C-deposition were 2.92 eV. The E_g was reduced by increasing In content in $In_xGa_{1-x}N$ [10,21]. In a similar result, Wagner et al. reported the composition dependence of the band gap energy of the strained $In_xGa_{1-x}N$ layers grown by MOCVD. The energy E_g of $In_xGa_{1-x}N$ decreased from 3.43 to 3.28 eV with the increasing in ratio from 0.02 to 0.15 [25]. The band gap values of n–Si was also found to be 1.12 eV. The electron affinities χ of p–InGaN and n–Si were 4.20 eV and 4.05 eV, respectively [6,24]. According to the band gap values of p–$In_{0.5}Ga_{0.95}N$ and n–Si (2.92 and 1.12 eV), the barrier ΔE_c for electrons was followed by $\Delta E_c = \chi_{p\text{–InGaN}} - \chi_{Si}$ and the barrier ΔE_v for holes was calculated by $\Delta E_v = E_{g(InGaN)} - E_{g(Si)} + \Delta E_c$ (Figure 2). As a result, the energy band diagram showed a small conduction band offset of 0.15 eV and a large valance band offset of 1.95 eV [22,24–26]. Therefore, the electrons' injection from n–Si into p–$In_xGa_{1-x}N$ will be easier than the holes' injection from p–$In_xGa_{1-x}N$ into n–Si because the energetic barrier ΔE_v of holes is many times higher than the barrier ΔE_c of electrons. With the existing space charge layer at the forward bias, the current is limited. However, the depletion width will decrease because of the low potential barrier, and the current will increase easily by increasing the voltage [6,27,28].

3.3. I–V Measurements

Figure 3 shows the current density–voltage characteristics of p–GaN/n-Si (device-A) and p–InGaN/n-Si (device-B) tested at RT based on a 1-mm^2 contact. The applied voltage of measurement was extended from −20 V to +20 V for both devices. The current densities and the leakage current densities are found in the area of 1 cm^2.

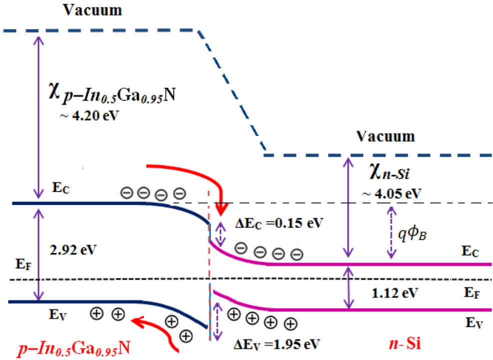

Figure 2. Energy band diagram of the p–$In_{0.5}Ga_{0.95}N$/n–Si hetero junction diode.

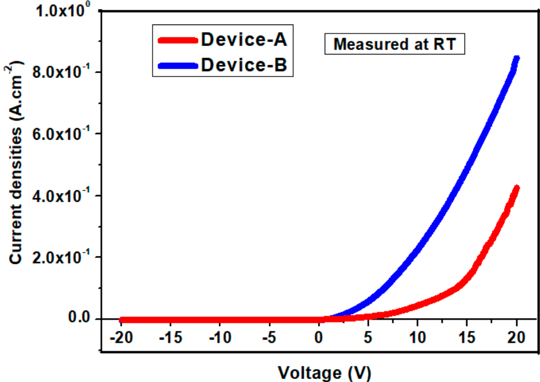

Figure 3. Current–voltage characteristics of p–GaN/n-Si and p–InGaN/n-Si diode, measured at room temperature.

At the bias range of (−5 V, +5 V), the leakage current of diodes at −1 V and the turn-on voltages at RT were 1.43×10^{-7} A, 1.5 V (device-A) and 2.58×10^{-7} A, 2.4 V (device-B). Our devices had an improvement in the turn-on voltage with the increase in content in the p–InGaN layer.

With the wide voltage of (−20 V, +20 V), Figure 3 also shows the breakdown voltage was beyond the largest instrument capacity of ~20 V for both diodes. The leakage currents also were found to be 9.31×10^{-7} and 3.38×10^{-6} A at −5 V for (device-A) and (device-B), respectively. At the forward bias of 20 V, the current densities of diodes were 0.421 and 0.814 A·cm^{-2} for device-A and device-B, respectively. Higher holes concentration in the p–InGaN layer with the performance of the in ratio in p–InGaN leads to the higher current density of device-B. In addition, with the high conduction of electrodes, the forward current of diodes increased rapidly at the bias of (−20 V, +20 V). The rectification ratio (on/off) of diodes were also found to be 3.22×10^4 (device-A) and 6.61×10^4 (device-B), respectively.

Figure 4 shows the semilogarithmic I–V characteristics of diodes under the forward bias, which were tested at the RT temperature. All parameters of diodes can be calculated by the thermionic-emission (TE) mode (for $qV > 3$ kT). They are given by the equations below [3,11,12].

$$I = I_0\left[\exp \frac{q}{nkT}(V - IR_s)\right] \quad (1)$$

$$\Phi_b = \frac{kT}{q} ln\left(\frac{AA^*T^2}{I_0}\right) \quad (2)$$

$$n = \frac{q}{kT}\left(\frac{\mathrm{d}V}{\mathrm{dln}I}\right) \quad (3)$$

$$A^* = \frac{4\pi qk^2m^*}{h^3} \quad (4)$$

where A^* is the effective Richardson constant, R_s is the series resistance, n is the ideality factor, I_o is the saturation current, q is the electronic charge, A is the area of diode, ϕ_b is the barrier height, m_e is the free electron mass, m^* is the effective electron mass, and h is the Plank constant [29–31]. In base Equation (4), the theoretical value of A^* was 26.4 A·cm^{-2}·K^{-2} for p–GaN (m^* = 0.22m_e), and 23 A·cm^{-2}·K^{-2} for p–InGaN (m^* = 0.19m_e) [6,12,13].

As shown in Figure 4, the barrier height of diodes can be calculated from I_o as the saturation current. Based on Equation (2), and from the plot of ln$I$ versus V, the saturation current I_o can be determined by intersecting the interpolated straight lines from the linear region with the current axis [12,20].

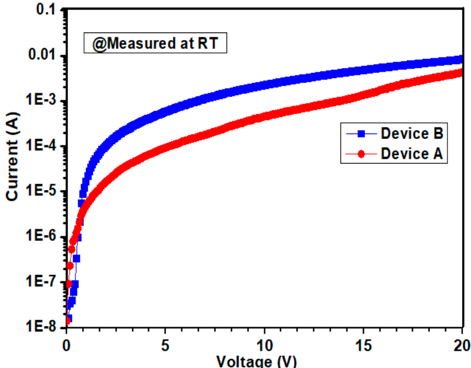

Figure 4. The I–V characteristics of device-A and device-A under the forward bias tested at room temperature.

Figure 5a,b show the semi logarithmic I–V characteristics of diodes were tested at the temperature range from 25 to 150 °C. From Figure 5, the leakage current of diode at −5 V increased from 9.39 × 10^{-7} A (device-A) and 3.38 × 10^{-6} (device-B) at 25 °C to 3.25 × 10^{-5} A (device-A) and 2.64 × 10^{-4} A (device-B) at 150 °C. Based upon Equations (1)–(3), the barrier height values were found to increase from 0.54 to 0.69 eV (device-A), and 0.50 to 0.62 eV (device-B), whereas the ideality factor n decreased from 5.9 to 4.8 (device-A), and 5.1 to 3.6 (devices-B) with testing temperatures ranging from 25 to 150 °C. These achieved parameters of diodes made by RF sputtering are similar to some previous works with the GaN-diodes made by MOCVD and techniques [1,3,18,28].

Similar to the analysis of the parameters for Schottky diodes, the effect of series resistance R_s will influence and change the ideality factor n. They can be determined by using Cheung's method. It is given by the equation below [13,32,33].

$$\frac{\mathrm{d}V}{\mathrm{d}(\ln I)} = \frac{nkT}{q} + IR_S \tag{5}$$

Based on Equation (5) and the plot of the dV/d(ln$I$) versus I from Figure 6, the series resistance R_s and ideality n can be calculated the from the the slope and the intercept [11,33,34]. Table 1 shows all detailed parameters of the I–V measurement for both devices tested at different temperatures. With the high Indium content, the R_s and n values of device-B were smaller than device-A. They showed 412 Ω and 5.3 at 25 °C and decreased them to 133 Ω and 3.8 at 150 °C.

By comparison, with Cheung's method, the modified Norde function was also used to define the effective barrier height of diodes. It is followed by the equation below [12,13,34–36].

$$F(V, I) = \frac{V}{\gamma} - \frac{kT}{q} \ln\left(\frac{I}{AA^*T^2}\right) \tag{6}$$

The effective barrier height ϕ_B is followed by the equation below.

$$\phi_B = F(V_{\min}) + \frac{V_{\min}}{\gamma} - \frac{kT}{q} \tag{7}$$

where the F(V_{min}) is the minimum value of F(V,I), γ is the first integer (dimensionless) greater than n, and V_{min} is the corresponding voltage at F(V_{min}).

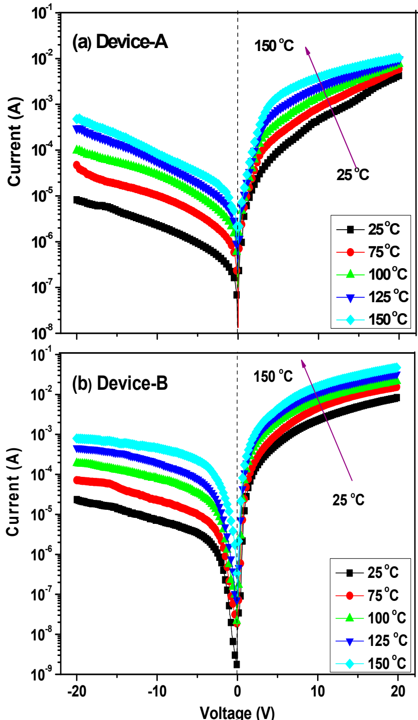

Figure 5. Forward and reverse (I–V) characteristics of (**a**) device-A and (**b**) device-B tested in the temperature range of 25–150 °C.

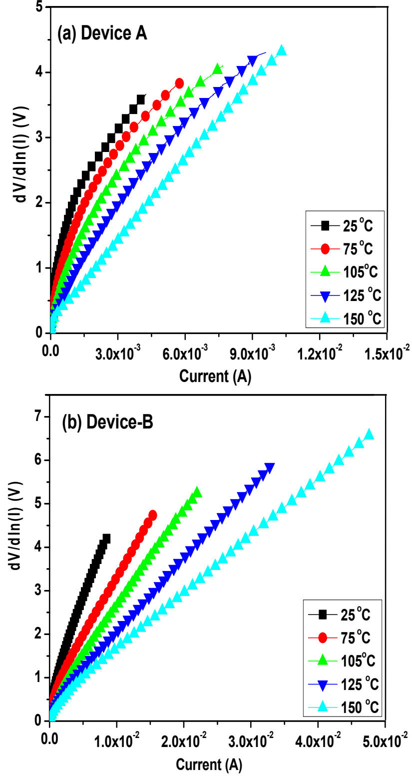

Figure 6. Plots of dV/dln(I) versus I for (**a**) device-A and (**b**) device-B tested in the temperature range of 25 to 150 °C.

Figure 7a,b shows the plot of F(*V*,*I*) versus *V* of hetero junction diodes as a function of the different temperatures tested. By using Equations (6) and (7), the barrier height values were determined to be 0.56 eV (device-A) and 0.53 eV (device-B) at 25 °C, and reached 0.71 eV (device A) and 0.64 eV (device B) at 150 °C (Table 1).

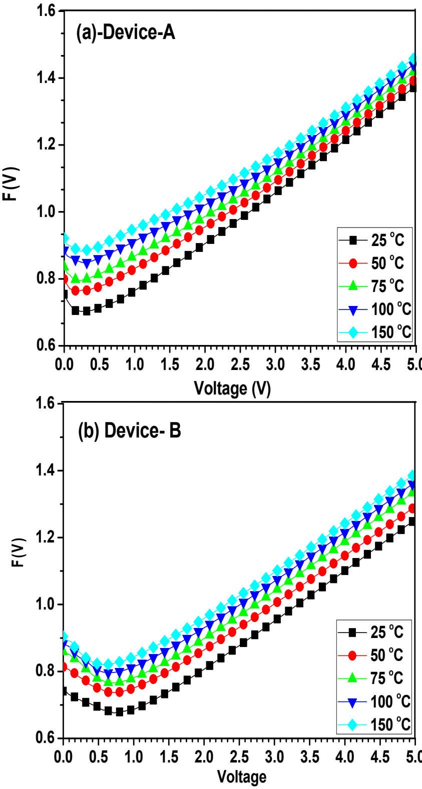

Figure 7. The $F(V)$ versus V plot for (**a**) device-A and (**b**) device-B tested in the temperature range of 25 to 150 °C.

4. Discussion

Table 1 showed the detailed comparisons of the *I*–*V* measurements for both hetero junction diodes. The smallest leakage current of 9.31×10^{-7} A at −5 V was found in device-A tested at RT, while the smallest turn-on voltage was ~1.5 V. The highest current density of 0.814 A·cm^{-2} were found in device-B at the forward bias of 20 V. At the reverse bias, the breakdown voltage of both devices was strongly blocked with the value at −20 V. The forward current increased quickly with the occurrence of the in content in the *p*–InGaN layer. With a higher holes carrier concentration of 2.53×10^{17} cm^{-3} and a smaller band gap of 2.92 eV, device-B showed the small turn-on voltage of 1.5 V, barrier heights of 0.5 eV (Cheung's method), and 0.53 eV (Norde method), compared with all parameters of device-A [20].

The ideality factor *n* of diodes decreased quickly, from 5.9 at 25 °C for device-A to 3.6 at 150 °C for device-B. For the Schottky diode, the turn-on voltage is often small, and the ideality factor *n* is <2 [2,3,13]. In our diodes, the ideality factors had high values because of the present high series' resistances, which were calculated from the slope of the linear region in Cheung's method. In addition, from the band diagram in Figure 2, the barrier ΔE_v for holes was larger than that of ΔE_c. Therefore, a higher valance band offset will have a high potential barrier, large turn-on voltage, high ideality factor, and high series resistance Rs. The high ideality factor of our diodes at RT also has been attributed to the high structural defect density, which serves as the trap-assisted generation-recombination centers. This procedure also influences the current transportation of hetero junction diodes [13,17,20]. The R_s values also reduced from 876 Ω at 25 °C (device-A) to 133 Ω at 150 °C (device-B). The generations of

series resistance, interface states, and the voltage drop across the interfacial layer caused the slight difference between the ideality factor n calculated from the ln$I$ vs V and dV/d(ln$I$) vs. I plots (Table 1).

Both hetero junction diodes had remarkable improvements as compared with some other homo and hetero junction diodes made by different techniques. Their deposition had epitaxial growth and was conducted at high temperatures above 800 °C by MOVCD [18,19,27,37–39]. Our devices had displayed the special I–V characteristics, which can be attributed to the low-temperature deposited at −400 °C without using a buffer layer. Both our diodes showed the breakdown voltage above 20 V for a 1 mm^2-sized contact.

Table 1. The parameters calculated from electrical characteristics of hetero junction diodes as a function of testing temperatures.

Temp (°C)	Leakage Current (A) at −5 V	Barrier Height ϕ_B (eV)		From I–V	Cheung's Function dV/dln(I) versus I	
		I–V	Norde	n	R_s (Ω)	n
Device-A						
25	9.31×10^{-7}	0.54	0.56	5.9	876	6.4
75	4.02×10^{-6}	0.57	0.58	5.6	683	5.8
100	1.03×10^{-5}	0.63	0.64	5.4	549	5.5
125	1.91×10^{-5}	0.66	0.68	5.0	467	5.3
150	3.26×10^{-5}	0.69	0.71	4.8	413	5.1
Device-B						
25	3.38×10^{-6}	0.50	0.53	5.1	486	5.3
75	9.92×10^{-5}	0.53	0.55	4.8	292	4.9
100	3.43×10^{-5}	0.57	0.60	4.6	233	4.7
125	7.81×10^{-5}	0.60	0.62	4.1	173	4.2
150	2.64×10^{-4}	0.62	0.64	3.6	133	3.8

K.E.F. Keskenler et al. made the n–ZnO/p–Si hetero junction diode by using a sol-gel spin technique [38]. The leakage current, barrier height, ideality factor, and series resistance of their diode were determined to be 4×10^{-6} A at −1 V, 0.71 eV, 2.03, and 42.1 Ω at RT. Chirakkara et al. investigated the n–ZnO/p–Si (100) diode by pulsed laser deposition without using a buffer layer [39]. By I–V testing at the temperature range of 300–390 K, the barrier height increased from 0.6 (300 K) to 0.76 eV (390 K). Seng et al. reported the n-ZnO/p-GaN diode formed by the RF technique [40]. Their diode had showed the turn-on voltage of 2 V, the leakage current of 1.6×10^{-5} A, and the series resistances of 102 Ω. Hsueh et al. investigated the n–$Mg_xZn_{1-x}O$/p–GaN hetero-junction diode. Their ideality factors decreased from 3.86 to 7.00, with testing temperature increasing from 25 to 125 °C [41]. Compared to our previous works, for the sputtering-made n–$In_xGa_{1-x}N$/p–Si devices with the similar area of 1-mm^2, the leakage current densities at −5 V were 5.96×10^{-5} A·cm^{-2} for n–GaN/p–Si and 2.81×10^{-4} A·cm^{-2} for n–$In_{0.4}Ga_{0.6}N$/p–Si, respectively [20].

At this time, there is rarely a report about the Mg-doped–$In_xGa_{1-x}N$ film made by RF sputtering below 400 °C deposition and designed diode on the n–Si wafer. With the improvement of doping Mg in $In_xGa_{1-x}N$ film, our devices had the stable I–V characteristics up to the testing temperature of 150 °C. The p–$In_xGa_{1-x}N$/n–Si diodes with the strong breakdown voltage of 20 V and leakage current of ~10^{-7} A will create the opportunity to develop the power devices.

5. Conclusions

p–$In_xGa_{1-x}N$/n–Si diodes were successfully investigated by directly depositing the p-GaN and p–Mg-doped-$In_{0.5}Ga_{0.95}N$ films on n–Si(100) wafers without using a buffer layer. The highest current density of 0.814 A·cm^{-2} at 20 V and the smallest turn-on voltage of 1.5 V were found for p–InGaN/n–Si devices. Pt and Al for Omhic contacts contributed to the high current density at the forward bias of hetero junction diodes. Both diodes also displayed the good I–V characteristics up to the testing temperature of 150 °C and the breakdown voltages of 20 V. By calculating the equations based on the TE mode as well as Cheungs' and Norde method, the obtained electrical parameters were also compared. They can be referred to develop cost-effective solutions in electronic devices.

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Conflicts of Interest: The authors declare no conflict of interest.

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